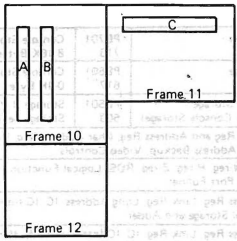


10A-A1 Console Clock and Communications Common to Console Stations A and B

					A
	PC411, 413 Sel Out Bypass	PC401, 403 Sel Out Bypass	PC581 Terminators	PC351 9 5419 MHz Osc	B
PC361-373	Clock Control, Cycle Count, Single-Cycle Control				C
PC475-479	Port Selection and Control, A-side or B-side				D
PC381-395	Port 0, 1 Selection, A-side and B side Port Funnels				E
					F
PC425-435	SR Bits 3-9, P to Ports 3, 4, W reg Bits 0-4, P to Ports 0, 1, 3, 4 and Conversion				G
PC441-450	SR Bits 3-9, P to Ports 0B, 5, W reg Bits 0-4, P to Ports 0B, 5, Metering Out to Director 1				H
PC451-460	SR Bits 3-9, P to Ports 0A, 6, W reg Bits 0-4, P to Ports 0A, 6, Metering Out to Director 2				J
PC461-470	SR Bits 3-9, P to Ports 2, 7, W reg Bits 0-4, P to Ports 2, 7, Metering Out to Director 3				K
PC471, 473	Port Receiver Card				L
PC501-509, 903	Console Communication Register				M
PC561-573	Conversion and Clocks				N
PC551-557	Battery Operated Clock, CR Timer, Power Off Timer				P
					Q
					R
					S
PC601-619	Modem Controls				T
PC621-619	Modem				U
					V

10A-B1 Console B Logic

PE751 763	Console Storage 16 24K Bytes	PE701 713	Console Storage 1 8 16K Bytes	A
PE801 813	Console Storage 24 32K Bytes	PE601 617	Console Storage 0-4K Bytes	B
PE651 667	Console Image Storage 4 8K Bytes (of Console Storage)	PE501, 503	Storage X-Y Decode, Storage Sel Control and IMPL	C
PE251 263	Image Storage Reg and Address Reg, Char Address Reg, Incrementer, and Character Address Backup, Video Controls			D
PE001 015	Storage Reg, W reg, H reg, Z reg, ROS, Logical Function, Local Storage, Port Funnel			E
PE101 115	Storage Address Reg, Link Reg, Long Address, IC, IC Interruption Buffer, Control Storage and Adder			F
PE121 135	Storage Address Reg, Link Reg, IC, IC Interruption Buffer, Intercommunication and Parity Predict Controls			G
PD601 615	Interruption Array, Interruption IC and Control			H
PD621 630	W reg, Count, IC, Indirect Reg Interruption Buffers, W reg Input and Funnel, Indirect Reg, XOR, Link Input AO			J
PE231 245	Operator Station and Controls, Keyboard Put and Take Regs and Controls			K
PE881 891	Read Control 1-3 for Diskette Drive, Take Funnel			L
PE861 873	Diskette Drive Write Controls			M
PE201 221	Link Register Funnel, Take Funnel, and Parity Generate			N
PD541 549	Console LED Controls and Checks, IMPL Interlocks			P
PE851 855	Diskette Drive Control Lines	PD561, 601	Interruption Controls	Q
PD431 437	Channel Communication Controls			R
PD459 469	Channel Communication Controls, Address Plug Bits			S
PD401 411	Channel Communication Controls			T
	PE831 Diskette Dr Ctrl			U
				V

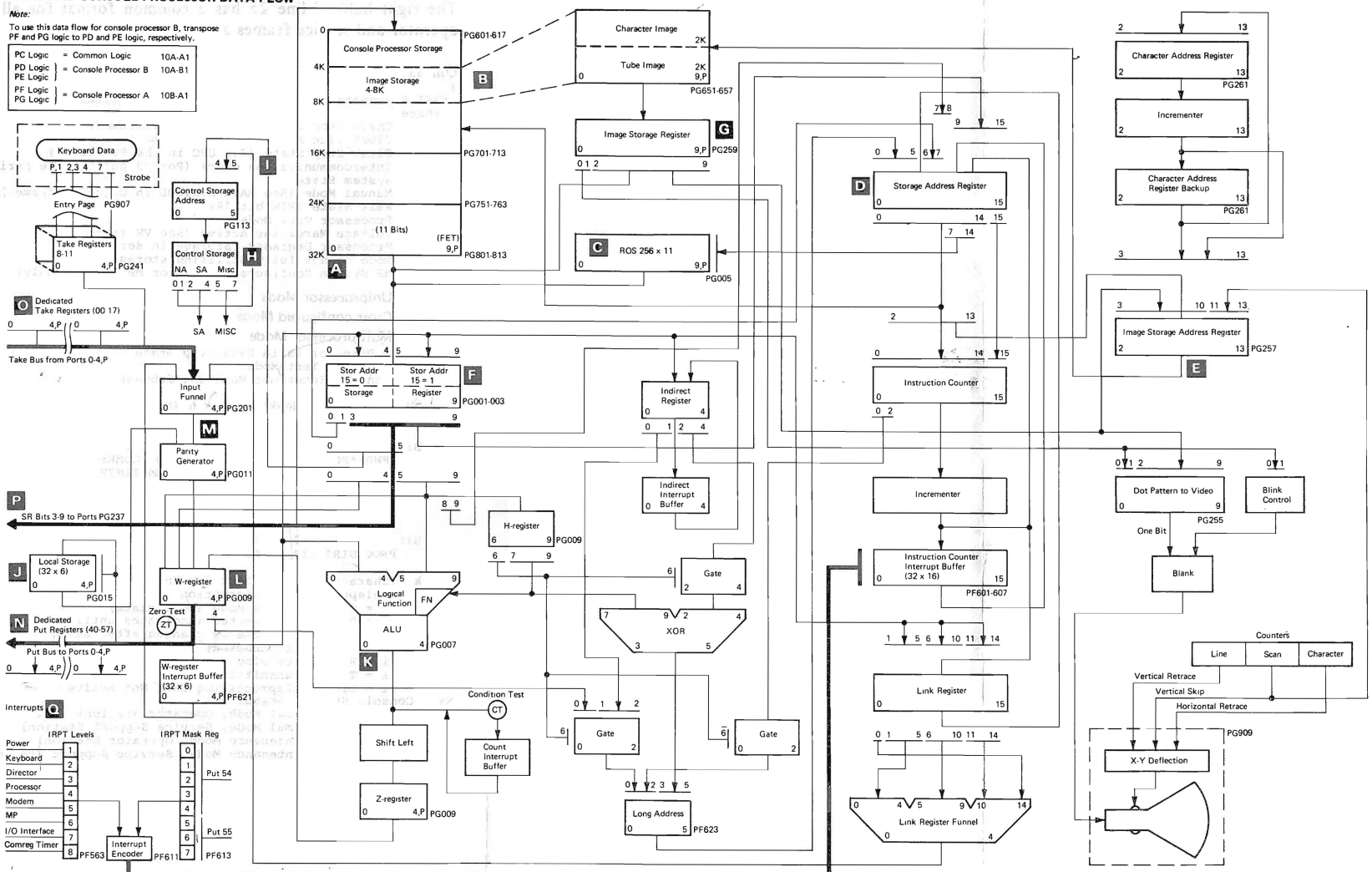
10B-A1 Console A Logic

PE751 763	Console Storage 16 24K Bytes	PE701 713	Console Storage 1 8-16K Bytes	A
PE801 813	Console Storage 24 32K Bytes	PE601 617	Console Storage 0-4K Bytes	B
PE651 667	Console Image Storage 4-8K Bytes (of Console Storage)	PE501, 503	Storage X Y Decode, Storage Sel Control and IMPL	C
PE251 263	Image Storage Reg and Address Reg, Char Address Reg, Incrementer, and Character Address Backup, Video Controls			D
PE001 015	Storage Reg, W reg, H reg, Z reg, ROS, Logical Function, Local Storage, Port Funnel,			E
PE101 115	Storage Address Reg, Link Reg, Long Address, IC, IC Interruption Buffer, Control Storage and Adder			F
PE121 135	Storage Address Reg, Link Reg, IC, IC Interruption Buffer, Intercommunication and Parity Predict Controls			G
PD601 615	Interruption Array, Interruption IC and Control			H
PD621 630	W reg, Count, IC, Indirect Reg Interruption Buffers, W reg Input and Funnel, Indirect Reg, XOR, Link Input AO			J
PE231 245	Operator Station and Controls, Keyboard Put and Take Regs and Controls			K
PE881 891	Read Control 1 3 for Diskette Drive, Take Funnel			L
PE861 873	Diskette Drive Write Controls			M
PE201 221	Link Register Funnel, Take Funnel, and Parity Generate			N
PD541 549	Console LED Controls and Checks, IMPL Interlocks			P
PE851 855	Diskette Drive Control Lines	PD561, 601	Interruption Controls	Q
PD431 437	Channel Communication Controls			R
PD459 469	Channel Communication Controls, Address Plug Bits			S
PD401 411	Channel Communication Controls			T
	PE831 Diskette Dr Ctrl			U
				V

SIMPLIFIED CONSOLE PROCESSOR DATA FLOW

Note:
To use this data flow for console processor B, transpose PF and PG logic to PD and PE logic, respectively.

PC Logic	= Common Logic	10A-A1
PD Logic / PE Logic	= Console Processor B	10A-B1
PF Logic / PG Logic	= Console Processor A	10B-A1



Line 25 Format

The right half of line 25 has a common format for all operator and service frames as follows:

```
COL 33
|
 KASI PSW=hhhhhhhh hhhhhhhh SMWTVPuDt hhh ki<xx>
  where:
    K = Check-Stop State (See OP or PT frame.)
    A = Clock Slue Active (See VM frame.)
    S = Clock-Stop State (See CPC in the PT frame.)
    I = Intercommunication Check (Port 3 put or take parity)
    S = System State
    M = Manual Mode (See RATE CONTROL in OP or PT frame.)
    W = Wait State (PSW bit 14)
    T = Processor Test Mode
    V = Voltage Margining Active (See VM frame.)
    P = Processor Degraded (Storage in serial
        mode or not fully utilizing storage)
    u = MP System Configuration (AP or MP complex only)
    u = Uniprocessor Mode
    x = Cross configured Mode
    m = Multiprocessor Mode
    D = A Director Is in Hard-Stop State
    t = Director Test Mode
  hhh = Console Interrupt Mask and Submask

                h (Mask)          h (Mask)

        --------------     -----------------
    Bit  0   1   2   3     0   1   2    3
        PWR KBD DIR PROC   TP  MP I/O  COMREG
                                COMM TIMER

                h (Submask)

        -----------------
    Bit  0    1    2    3
       PROC DIR1 DIR2 DIR3

    k = Character of the Last Key Entered
    i = Teleprocessing Information
        i = C     Control Mode (Idle state)
        i = D     Disconnected (Indicates until
                  the frame is changed after being
                  disconnected)
        i = R     Receiving
        i = T     Transmitting
        i = blank Teleprocessing Link Not Active
xx - Console Station Status
        xx = NO (Normal Mode, Operator Station)
        xx = NS (Normal Mode, Service Support Station)
        xx = MO (Maintenance Mode, Operator Station)
        xx = MS (Maintenance Mode, Service Support Station)
```

Code	*SEQ Indicator*	*Meaning*
0	–	Successful load of tracks 0 and 1
1	4	Unsuccessful branch to 24K addressing (SAR bits 0-2 not equal to 110)
2	3	Cannot read track 1
3	3, 4	No diskette mounted (not ready)
4	2	Security key off
5	2, 4	Cannot read track 0
6	2, 3	Start looking for index
7	2, 3, 4	Start looking for strobe (read data ready)

The following codes are presented by the processor interrupt routine, and are valid when check stop (a K displayed in front of PSW =) is indicated on line 25.

Code	*SEQ Indicators*	*Meaning*
3	3, 4	Interface check
5	2, 4	Stop on check is active and not overridden
6	2, 3	CR14 parity check, byte 0
7	2, 3, 4	CR14 parity check, byte 1, or prefix register parity check (AP and MP only)
8	1	Absolute mode or double machine check and CR14 bit 0 = 1
9	1, 4	PSW bit 13 = 0 and conditions = no retry; or soft machine-check interrupt (MCI) occurred with PSW bit 13 = 0
A	1, 3	When the cyclic program counter has decremented to 0, the clocks are stopped in the processor, the console receives a processor interrupt, and the bezel indicator MASTER CHECK turns on
D	1, 2, 4	No valid machine-check (MC), advance during extended logout and CR14 bit 0 = 1
E	1, 2, 3	No valid MC advance during status logout and CR14 bit 0 = 1

Sequence Indicator	Binary Value
Seq 1	8
Seq 2	4
Seq 3	2
Seq 4	1

CONSOLE CONFIGURATION - NORMAL

3036 Interface and PORT Connections

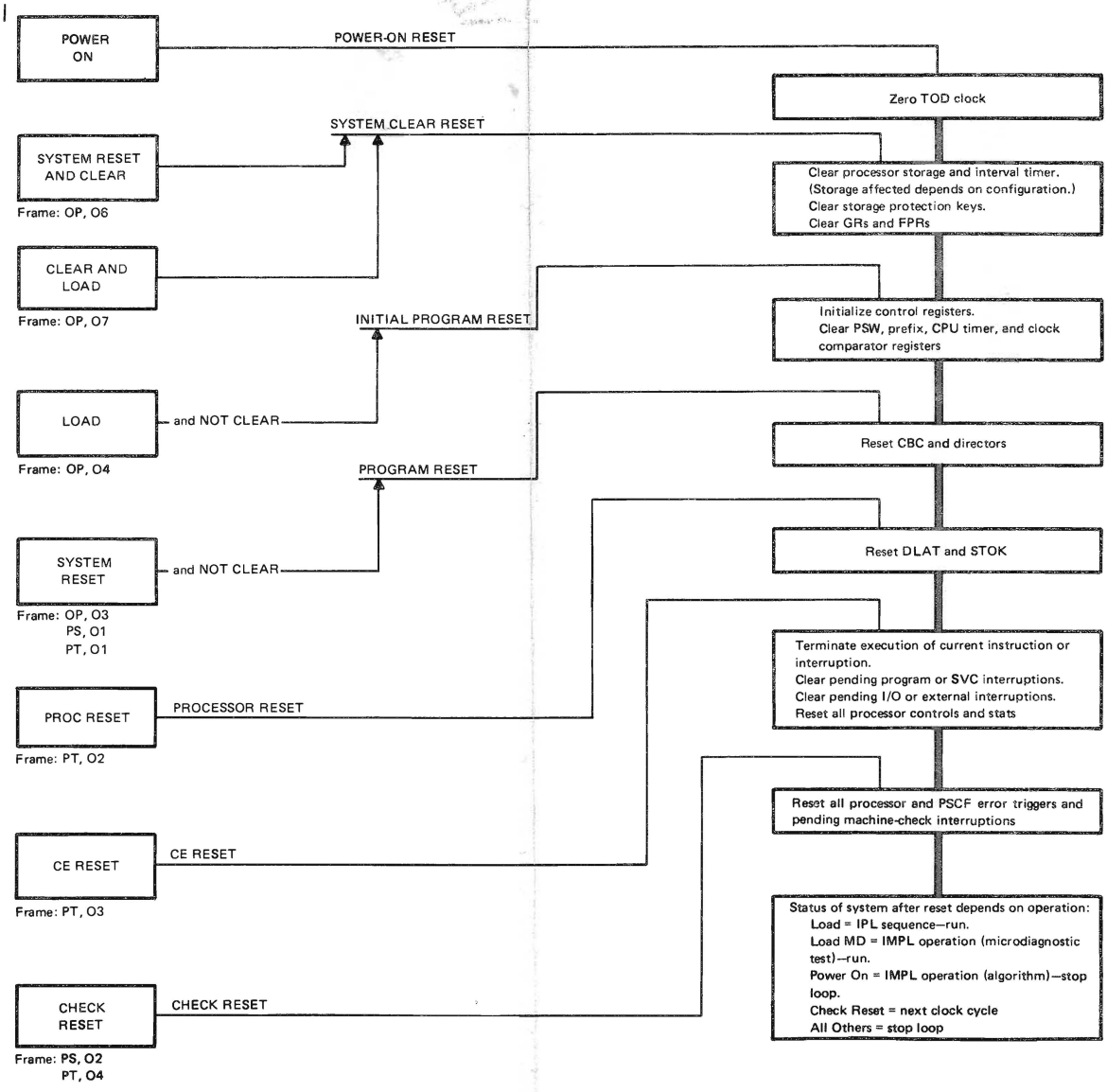
V-Gate

1	Bus In	CSI 'B'
2	Tag In	
3	Bus Out	
4	Tag Out	
5	Bus In	CSI 'A'
6	Tag In	
7	Bus Out	
8	Tag Out	
9		Unused
10		
11		
12		
13		
14	PORT #5	Director #1
15	PORT #6	Director #2
16	PORT #7	Director #3
17	PORT #3	Processor
18	PORT #4	Trace and MP or AP

W-Gate

Power Control (PORT - 2)

1	
2	
3	
4	FR04 - Processor
5	FR-15 PDU
6	FR05 Director


POWER ON
POWER-ON RESET
Zero TOD clock
SYSTEM CLEAR RESET
SYSTEM RESET AND CLEAR
Frame: OP, O6
Clear processor storage and interval timer.
(Storage affected depends on configuration.)
Clear storage protection keys.
Clear GRs and FPRs
CLEAR AND LOAD
Frame: OP, O7
INITIAL PROGRAM RESET
Initialize control registers.
Clear PSW, prefix, CPU timer, and clock comparator registers
LOAD
and NOT CLEAR
Frame: OP, O4
Reset CBC and directors
PROGRAM RESET
SYSTEM RESET
and NOT CLEAR
Frame: OP, O3
PS, O1
PT, O1
Reset DLAT and STOK
Terminate execution of current instruction or interruption.
Clear pending program or SVC interruptions.
Clear pending I/O or external interruptions.
Reset all processor controls and stats
PROC RESET
PROCESSOR RESET
Frame: PT, O2
Reset all processor and PSCF error triggers and pending machine-check interruptions
CE RESET
CE RESET
Frame: PT, O3
Status of system after reset depends on operation:
Load = IPL sequence—run.
Load MD = IMPL operation (microdiagnostic test)—run.
Power On = IMPL operation (algorithm)—stop loop.
Check Reset = next clock cycle
All Others = stop loop
CHECK RESET
CHECK RESET
Frame: PS, O2
PT, O4

CONSOLE STATIONS CONFIGURATIONS

Refer to TODM Volume 6, Chapter 2.

The console can be in either of two modes, normal or maintenance, and a console station can perform either of two functions: operator or service. The console mode and station function are combined to define the state of a console station.

The console station states are:

<NO> – Normal mode, operator function. The station is the operator station, which communicates with the operating system and controls the system power.

<NS> – Normal mode, service function. The station is used to perform service on system components and to perform manual operations (such as system reset, IPL, and control store load). The station monitors system components and records trace events and logouts.

<MO> – Maintenance mode, operator function. The station performs all the functions described under <NO> and <NS> states.

<MS> – Maintenance mode, service function. The station is used to perform service on the channel directors or trace unit. The station is considered to be offline to the console and, as such, may itself be serviced.

The console station state is displayed on the right half of line 25.

In normal mode, one station is in <NO> state and the other station is in <NS> state. In maintenance mode, one station is <MO> state and the other station is in <MS> state. Any other combinations are invalid.

Configuration and Port Assignments

<NO> – The station is assigned ports 0 and 2.

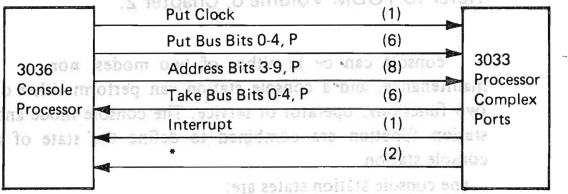
<NS> – The station is assigned port 0; ports 3 and 4 (if the processor is powered up); and ports 5, 6, 7 (for Directors 1, 2, and 3, respectively, if powered up).

<MO> – All ports are assigned, except one of ports 4-7, which may be assigned to the <MS> station.

<MS> – Port 0 and one of ports 4-7, which may be assigned from the <MO> side, are assigned.

PORT ALD LOGIC REFERENCE

Refer to TODM Volume 6, Chapter 1.



Port 2 from Console

PDU adapter	WJ100
Processor adapter	WJ101
Director adapter	WJ102
Service processor	WJ103

Port 2 to Console

PDU adapter	WJ200
Processor adapter	WJ300
Director adapter	WJ400
*Power good	WL200

Ports 5, 6, and 7

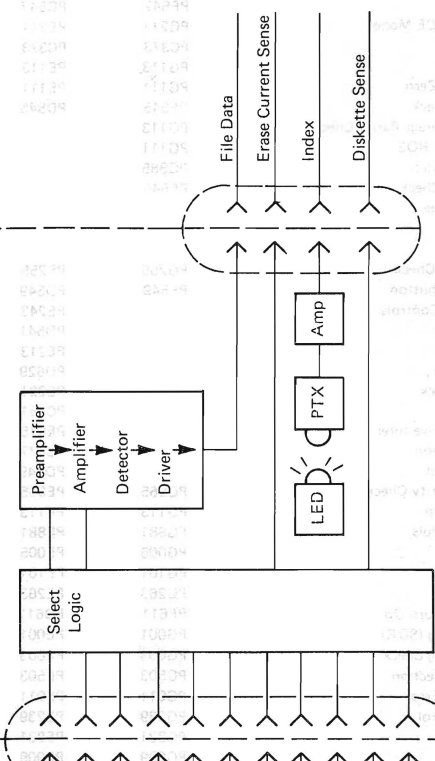
From console	WL510
To console	WL500

Port 4

From console	WL111
To console	WL113

Port 3

From console	WL300
To console	WL310
*Run meter	WL310
*Gross error	WL310


Write Data
Upper Tracks
Write Gate
Select Head
Erase Gate
Switch Filter
Access 0
Access 1
Access 2
Access 3
Head Engage
Exit PE915 and PG915
Select Logic
Preamplifier
Amplifier
Detector
Driver
LED
PTX
Amp
File Data
Erase Current Sense
Index
Diskette Sense
Entry PE915 and PG915

Line Name	*Sup A*	*Sup B*
Access Lines	PG873	PE873
Active Interrupt Cycle	PF611	PD611
Block Interrupt	PF611	PD611
Branch and Link Op	PG113	PE113
Carry Out of Incrementer	PG121	PE121
CE Mode	PF547	PD547
Microcode CE Mode	PG211	PE211
Clocks	PC373	PC373
CSA	PG113	PE113
CSA 0 3 = Zero	PG111	PE111
Console Check	PF545	PD545
Control Storage Parity Check	PG113	PE113
Fetch from ROS	PG111	PE111
First Bit Latch	PG885	PE885
Hardware Check	PF545	PD545
Head Engage	PG873	PE873
Index	PG873	PE873
Interrupts	PF601	PD601
ISR Parity Check	PG255	PE255
IMPL Pushbutton	PF549	PD549
Keyboard Controls	PG243	PE243
LED Check	PF541	PD541
LEDs	PG213	PE213
Link Check	PF629	PD629
Master Check	PG221	PE221
Oscillator	PC351	PC351
Diskette Drive Intercommunications	PG915	PE915
Port Selection	PC477	PC477
Power Good	PF549	PD549
Put Reg Parity Check	PG865	PE865
Put Tape Op	PG113	PE113
Read Controls	PG881	PE881
ROS	PG005	PE005
SAR	PG101 123	PE101-123
SAR Check	PG263	PE263
Special Return Op	PF611	PD611
Storage Reg (SDR)	PG001	PE001
Storage Reg Check	PG003	PE003
Storage Selection	PG503	PE503
Take Reg Error	PG011	PE011
Tube Control	PG239	PE239
VFO	PG831	PE831
W-reg	PG009	PE009
W-reg Parity Check	PG211	PE211
Write Controls	PG871	PE871

CONSOLE AIDS

Tie Ups

The tie up is to the D08 ground pin.

Board 10AA1 tie ups:
To tie port 2 to SUP, ground the following pins:
Port 2 to A side = D2D10
Port 2 to B side = D2M2

Tie ups in SUP:

Function	*Pin 10BA1, Console A 10AB1, Console B*	*ALD Page*
Tie off file data check	L2J11	PE/PG889
Tie off master check	N2U06	PE/PG221
Tie off hardware check	P2P12	PD/PF545
Tie off console check	N2D02	PE/PG221
Disable IMPL on check	P2U05	PD/PF549
Tie off power check	Q2G12	PD/PF563
Inhibit interrupt priority	H2U10	PD/PF563
Block all interrupts	Q2J10	PD/PF561
Block interrupts level 1	H2M05	PD/PF609
Block interrupts level 2	H2P06	
Block interrupts level 3	H2P07	
Block interrupts level 4	H2G13	
Block interrupts level 5	H2M02	
Block interrupts level 6	H2M03	
Block interrupts level 7	H2J13	
Block interrupts level 8	H2P02	
IPC timer tie off	11CA1-S2G10	YD409

ALD References

Logics for SUP console A are PFxxx and PGxxx.
Logics for SUP console B are PDxxx and PExxx.

Diskette drive intercommunications are on ALD pages PE/PG831, 915, and 917.

LEDs are on ALD pages PE/PG213 and 221.
Error LEDs are on ALD pages PD/PE543 and 545.

ERROR-INDICATOR PANEL

Console Processor Error-Indicator Panel

The console processor error-indicator panel (hand-held) is located inside the door on the left-hand side of the control panel. The top half of the indicator panel (physical assignment) is for station A; the bottom half is for station B.

EARLY ERROR

Denotes a parity error that occurs at the beginning of storage time.

ISR: Image storage register error.

LINK: Link register error.

W REG: W-register error.

DISK: Put register 58 or 59 error. The put registers contain diskette drive commands.

A IMPL OR B IMPL: Indicates to the other station that an error IMPL, a pushbutton IMPL, or a remote IMPL is in process.

LATE ERROR

Denotes a parity error occurring at the end of storage time.

CS CHK: Control storage error.

SAR: Storage address register error.

TAKE: Error in any take register 0-7 or 10-13.

Bottom Row Indicators

The bottom row of indicators changes dynamically and is "frozen" when an error occurs.

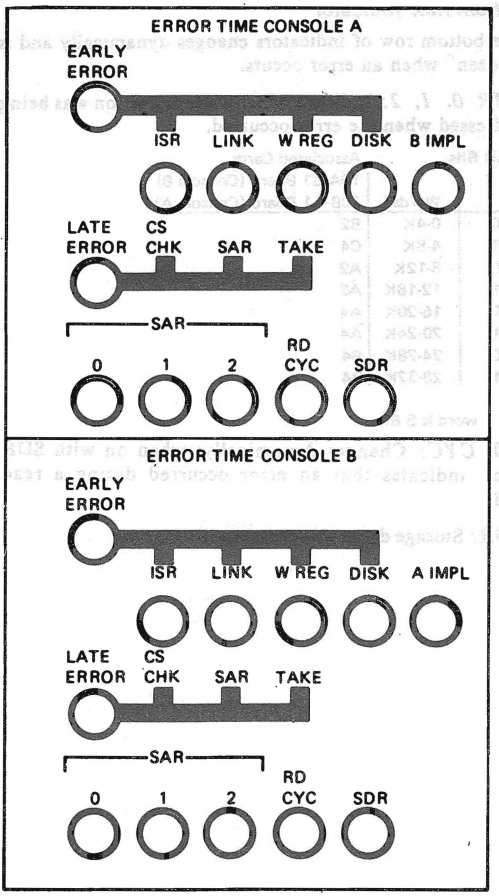
SAR 0, 1, 2: Indicate which storage section was being addressed when the error occurred.

SAR Bits		Associated Cards
0 - 2		10A-B1 Board (Console B)
	Words*	10B-A1 Board (Console A)
000	0-4K	B2
001	4-8K	C4
010	8-12K	A2
011	12-16K	A2
100	16-20K	A4
101	20-24K	A4
110	24-28K	B4
111	28-32K	B4

* A word is 5 Bits

RD CYC: Changes dynamically; when on with SDR error, indicates that an error occurred during a read cycle.

SDR: Storage data register error.



Error-Indicator Panel

53FD OPS

Read

1. Wait for index to generate FILE READY take 18 bit 4.
2. Engage file head. Put 59 bit 3. Heads are initially selected by put 58 bit 0; bit off is head 0, front, for even tracks; bit on is head 1, rear for odd tracks.
3. Seek op? Assess lines set 5ms put 58.
4. Wait for index take 18.
5. Set hi gain 1.6ms put 58.
6. Data from file sets first bit latch.
7. 5 bits assemble to set 'shift reg full' and 'set read buffer'
8. Read buffer full generates strobe
9. Wait for strobe take 18
10. Data in read buffer taken from take bus take 19
11. Waits for strobe

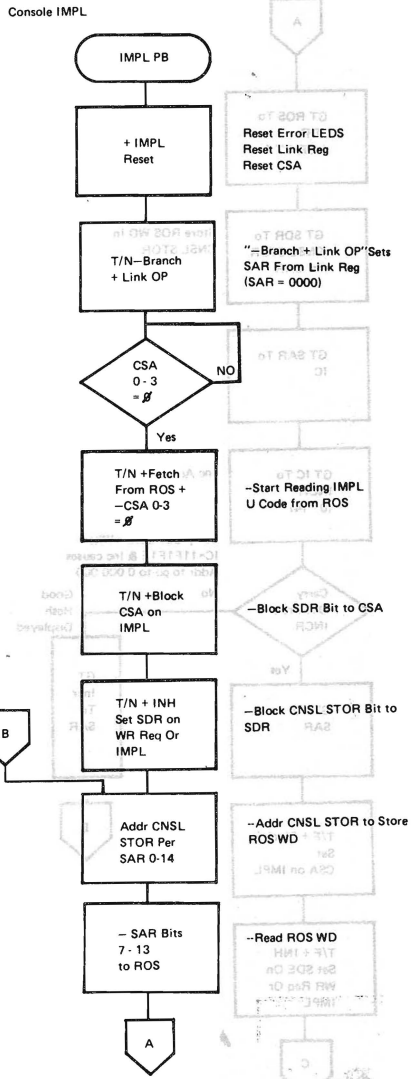
IMPL

1. Link reg reset to 0
2. CSA is reset to 0
3. SAR set to 0 from link reg by gate branch and link op
4. CSA 0-3 = 0 brings up:
   a. fetch from ROS
   b. block set CSA on impl to stop SDR 0, 1, 2, 3 setting CSA
   c. inhibit set SDR or WR reg on IMPL to stop MS data being read out to SDR.
5. SAR 0-14 addr main store
6. SAR 7-14 addr ROS
7. ROS data to SDR
8. SDR to main store
9. SAR 0-15 to the IC
10. IC to the incrementer
11. Incrementer to link reg
12. Link reg to SAR
13. Repeat 5-12 until SAR is equal to 1F 1F 1E
14. Incr. +2 brings on 'Carry out of incr.' SAR now = 0
15. 'Carry out of incr.' reset gates 4A, 4B, 4C
16. MS data from SAR 0 to SDR

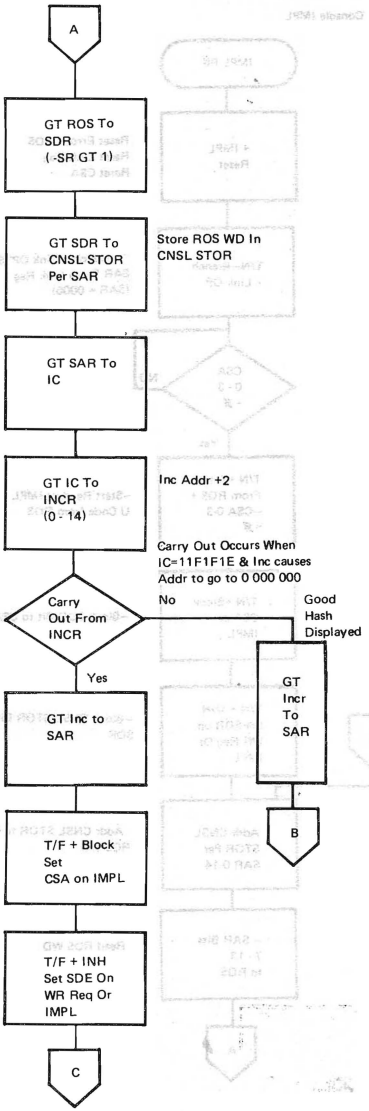
IMPL (continued)

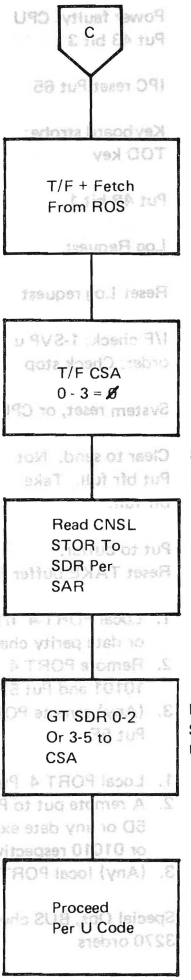
17. SDR 0, 1, 2, 3, to CSA for executing first instruction
18. As per IMPL listing, or refer to IMPL BOOTSTRAP
19. Data is loaded from disc tracks 0 and 1 into MS 000000 to 17 1F 1E
20. Branch and link to 100000 to execute disc IMPL code

FLOWCHART


Console IMPL
IMPL PB
+ IMPL Reset
Reset Error LEDS
Reset Link Reg
Reset CSA
T/N–Branch + Link OP
"–Branch + Link OP" Sets SAR From Link Reg (SAR = 0000)
CSA 0 - 3 = ø
NO
Yes
T/N +Fetch From ROS + –CSA 0-3 = ø
–Start Reading IMPL U Code from ROS
T/N +Block CSA on IMPL
–Block SDR Bit to CSA
T/N + INH Set SDR on WR Req Or IMPL
–Block CNSL STOR Bit to SDR
B
Addr CNSL STOR Per SAR 0-14
–Addr CNSL STOR to Store ROS WD
– SAR Bits 7 - 13 to ROS
–Read ROS WD
A

CONSOLE IMPL FLOW (continued)





Note 1 SAR 0-14 to ADDR CNSL STOR Fetch 1st Inst. SAR 5, 6, 8-13 Addr. ROS But not Fetch From ROS Blocks ROS Outgate.

INTERRUPTS

1.	Power	Set:	Power faulty; CPU Put 43 bit 3
		Reset:	IPC reset Put 65
2.	Keyboard	Set:	Keyboard strobe; TOD key
		Reset:	Put 4B bit 1
3.	Director	Set:	Log Request
		Reset:	Reset Log request
4.	CPU	Set:	I/F check; 1-SVP u order; Check stop
		Reset:	System reset, or CPU
5.	Modem	Set:	Clear to send. Not Put bfr full. Take bfr full.
		Reset:	Put to buffer. Reset TAKE buffer full
6.	Multi Proc (In local Processor)	Set:	1. Local PORT 4 I/F address or data parity check 2. Remote PORT 4 Put 5C = 10101 and Put 5D = 01010 3. (Any) remote PORT 4 Put 5F
		Reset:	1. Local PORT 4 Put 6B Bit 2 2. A remote put to PORT 4 Put 5C, 5D or any date except 10101 or 01010 respectively 3. (Any) local PORT 4 Take 1F
7.	CSI	Set:	Special Ops, BUS check 3270 orders
		Reset:	Reset I/F sequence
8.	Comreg or SVP Timer	Set:	Put 4B bit 3, SVP time out
		Reset:	Take 07, Put 45

Setting Mask

Put 55	Bits 3, 4 = 00 = Set Mask

	0	1	2	3	4
Put 55	6	7	8	0	0
Put 54	1	2	3	4	5

Setting Address

Put 55	Bits 3, 4 = 01 = Set Address
Put 55	Bits 0, 1, 2 = Level

000	Level 1
001	Level 2
010	Level 3
011	Level 4
100	Level 5
101	Level 6
110	Level 7
111	Level 8

Put 54	11	12	13	14	15
Put 54	6	7	8	9	10
Put 54	1	2	3	4	5
Put 54	—	—	—	—	0

OP Console Status

P	Parity
0	Attention
1	Not Used
2	Status Modifier
3	Busy
4	Channel End
5	Device End
6	Unit Check
7	Not Used

OP Console Sense

P	Parity
0	Command Reject
1	Not Used
2	Bus Out Check
3	Equipment Check
4	Data Check
5	Unit Specification Check
6	Not Used
7	Operation Check

Attention Identifier (AID)

7D	Enter Key
70	Alter Key
6E	Cancel Key
F1-F0	1 Thru 0
7A-7C	Program Function Keys

OP Console Commands
Write and Erase Write

Modifier Bytes That Can Be Included In Data Streams

10	SF	Start Field
11	SBA	Set Buffer Address
13	IC	Insert Cover
3C	RA	Repeat to Address
12	EUA	Erase Unprotected to Address
05	PT	Program Tab
15	NL	New Line
19	EM	End Message
1C	DUP	Duplicate
1E	FM	Field Mark

OPS Console Commands (3277)

00	TIO	
01	Write	WCC Modifies
02	Read Buffer	
03	No-op	
04	Sense	
05	Erase/Write	WCC Modifies
06	Read Modified	
0B	Select	
0F	Erase Unprotected	
E3	Sound PDU/CDU Alarm	
E4	Sense I/O	
07	Copy	Not Recognized On
0A	Diagnostic Read	Program OPS
09	Diagnostic Write	Console

WCC BYTE

5. Sound Audible Alarm
6. Restore Keyboard
7. Reset Modified Data Tag Bits

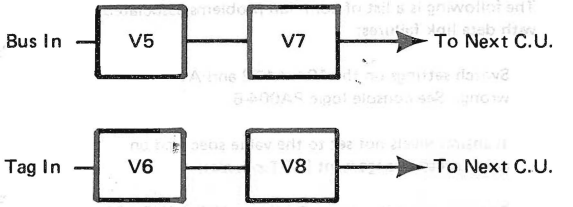
SRF Commands

4A	RDCPULG	One Log Sent
86	RDIRHD	All Director headers Sent
11	DIRLOG	0. Multiple Logs 1 - 3. 4 - 7. Dir Logs ID
8A	RDILOG	One Log Sent
3E	RDTRCLU	191 Trace Lines Description Sent
9E	RDERR	Error Triggers Sent
52	RDFRMNO	No of Frames Being/To Be Sent
5E	RDSSR	SSR Info Returned
65	WRCETRK	Write On CE Track of Disc. 2K Max
F2	RDCETRK	Read From CE Track
FE	RDCPUID	CPU ID Sent

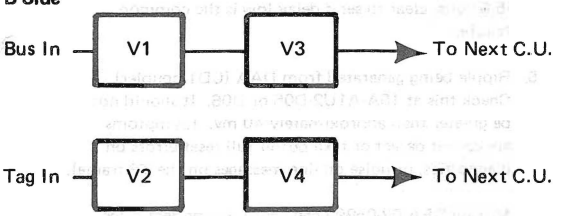
1D	Event	0-7. Event No...(00-Old) OC-New 8. Multiple Events 9-11. 12. Trace 13. CPU Log 14. Dir Logs 15. PWR Event
2A	RDEVENT	Specified Event Is Sent
26	RDEVTHD	All Event Headers Sent
46	RDCPUHD	CPU Log Headers Sent
09	CPULOG	0. Multiple Logs 1-3. 4-7. Log No.

CONSOLE INTERFACE

A Side



B Side



G.B.

3036 Modem Problem Checklist
For Data Link Failures

The following is a list of common problems associated with data link failures:

1. Switch settings on the 10A-A1T2 and A1U2 card wrong. See console logic PA004-6.

2. Transmit levels not set to the value specified on data access arrangement (CDT coupler).

3. Too much ripple on the -5 volts at 10A-A1U2-B06 (Approximately 90 mv is normal).

4. -5 volts supply out of specification. If more than -5.6 volts, clear to send delay low is the common failure.

5. Ripple being generated from DAA (CDT coupler). Check this at 10A-A1U2-D05 or D06. It should not be greater than approximately 40 mv. (Symptoms are carrier detect or take buffer full reset errors on diagnostics, or noise on line messages on the TP frame).

6. Missing REA 02-05992 can cause the modem diags to fail with take buffer full reset and data wrap errors. This REA is picked up on EC 275452.

IMPL Description

1. "Error IMPL's" usually affect only one station. If possible, display the error from the hand-held indicator panel or the take 0D-0F data on the IMPL or MC/PC frames. With this information, go to the troubleshooting flowcharts (Step 1) and swap cards using the error indicator charts. If both sides fail, suspect the -4 volts supply. Do not overlook the possibility of a bad diskette.

2. "Directed IMPL" occurs when code hangs in one side or the other due to inability to communicate through the comreg to the other station within its allotted time.

   a. 3033 failing station displays 'other station has assumed all functions'.
   b. 3031 failing station indicates IMPL = DEAD.
   c. Suspected cards = 10A-A1M2, 10A-B1Q2, 10B-A1Q2, 10A-A1C2.